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Development of RF MEMS cantilever beam to maximize capacitance in an activated state

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Abstract

This paper presents a simple design of planar cantilevers to be used in RF MEMS switches with reduced dielectric charging. It has been achieved by locating a DC biasing pad aside of RF line and dielectric insulator, while usually insulator is placed between grounded cantilever and DC pad with an applied potential. This, after a certain threshold voltage value, can lead to the effect of dielectric charging. Thus, after releasing the DC voltage, parasitic electric force can hold cantilever at the maximum capacitance position, which will require additional design complications to overcome this phenomena.

We investigated a cantilever design with a minimum contact area and capacitance close to the maximum with a separated activation electrode. Activation method is electrostatic. Final geometry along with simulation results are presented.

Keywords: cantilever, dielectric charging, RF MEMS, transient mechanical, variable capacitance.

INTRODUCTION

Radio-frequency microelectromechanical systems (RF MEMS) are promising devices to be used in switches instead of semiconductor-based devised providing low insertion loss, large off-state isolation, high power handling capabilities and better linearity [1]. Capacitive RF MEMS switch can be schematically presented as two layers of metallization separated by the layer of dielectric insulator with thickness d and an air gap h. The capacitance of a parallel plate capacitor with 2 dielectric layers is described as

$$C = \frac{\varepsilon_0 S}{h+\frac{d}{\varepsilon}}, \quad (1)$$

where $\varepsilon 0$ is vacuum permittivity, ε – is a permittivity of a dielectric insulator, S – plates surface.

Thus, if potential V is applied between plates, an electrostatic force (2) attracts plates reducing h and increasing capacitance, which maximum will be achieved when plates are separated only by the insulator layer (pull-in state).

$$F = \frac{V^2 \varepsilon_0 S}{2(h+\frac{d}{\varepsilon})^2}. \quad (2)$$

If DC voltage is applied directly through the insulating dielectric, in pull-in state one of the most important RF MEMS reliability problems occurs. Charges are injected in the dielectric film from the metal electrodes under the presence of high electric fields, which values should be higher than 1 MV/cm [2]. Distributions of charges in the dielectric will lead to the undesirable electric field during the discharge process, which will cause adhesion of cantilever to the insulator. To overcome this problem, for example, a complicated anchoring beams optimization can be made to reduce the pull-in voltage [5] or different insulating materials and thicknesses can be investigated [4].

We propose the cantilever – biasing electrode system to overcome the dielectric charging phenomena by separating the control electrode from the insulator. Therefore, the cantilever geometry is optimized to achieve the maximum capacitance switch coefficient with the reduced applied voltage by introducing the system of mechanical supports for the smooth attraction force distribution along the contact cantilever surface.

CANTILEVER DESIGN

It is possible to combine control and capacitive electrodes. In this case, the maximum capacitance will be determined by the roughness of the insulator and cantilever. However, in this case, there are two drawbacks. First is charging of dielectric insulator, which separates control electrode and cantilever, due to the applied biasing DC voltage. Second is the need to apply a voltage to the signal line and therefore to use a bias tee to supply this voltage which will occupy an additional space and affect the characteristics.

To reduce the dielectric charging, it is possible to use structures with a minimum activation voltage. However, soft designs will suffer from sticking with dielectric both in the manufacturing

process and during an operation. Figure 1 presents the proposed design of the cantilever for low-voltage operations, which is designed to avoid sticking with an insulator.

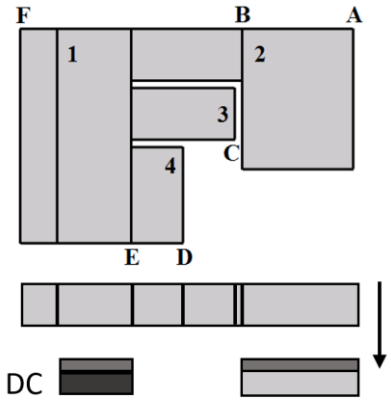

Figure 1: Cantilever profile geometry from the top view (top, 1 - Acting Area, 2 – Capacitance area, 3.4 – Support area) and side view (bottom)

The fixed end of the cantilever is on the left side (F). This is an anchoring area with fixed constraints. The free end of the cantilever is on the right side (A). The capacitance is formed by the area (2) and the bottom metallization. A DC voltage is applied between the area (1) and the DC pad under this are at bottom metallization. Areas (3) and (4) are intended for cantilever mechanical support. The main idea is that with the help of supports (3) and (4) the area (2) is evenly pressed against the bottom electrode, and the area (1) does not touch the DC electrode.

DISPLACEMENT SIMULATIONS

To illustrate this idea, this cantilever model has been designed and simulated. Cantilever deformations and the capacitance between it and the bottom metallization area were simulated for the different values of applied biasing DC voltage using finite elements method. Contact was modelled by the penalty barrier method [5]. The model material and geometry parameters were chosen as follows. Material is Copper (E=110 GPa, ν=0.35), cantilever thickness is 1 μm. The air gap thickness is 1 μm. Insulator over bottom metallization with a thickness of 0.2 μm is a silicon nitride (Si3N4) with ε=7. Optimized geometry parameters of cantilever areas are listed in Table 1. The deformation dependencies of the simulated cantilever are shown in Fig. 2.

Table I: Designed cantilever geometric parameters

Area #	Height, mm	Width, mm
1	145	50
2	95	75
3	35	70
4	65	35

The contact of the edge (A) occurs at a voltage of 10.7 V while the stiffness of the cantilever increases to kA. Then at a voltage of 12.3 V and 12.9 V -edges (C) and (D) respectively, the contact occurs and the stiffness increases to kC and kD respectively. At 14.3 V edge (B) reaches a contact and the area (2) is completely pressed to the bottom electrode. This is the state of the maximum capacitance. Further voltage increase leads acting area (1) to collapse.

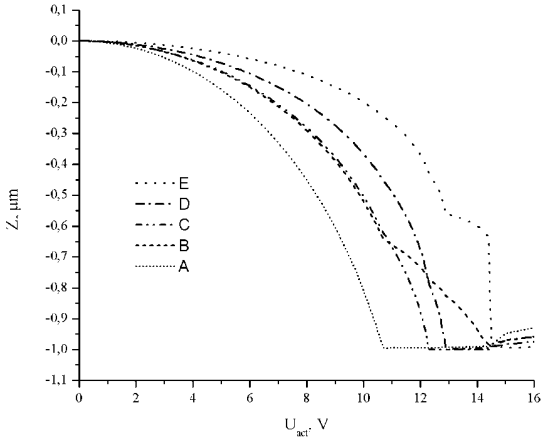

Figure 2: Deformation of the simulated cantilever edges depending on the applied voltage.

The dependence of the capacitance on the applied voltage has also been simulated (Fig. 3), where C0 is a capacitance without an applied voltage. The capacitance plot does not show a monotonic growth and has a clear maximum due to the variable cantilever stiffness increasing with each contact. Minimum (@0 V) capacitance is 0.066 pF maximum (@14.3 V) capacitance is 2.11 pF which leads to the capacitance ratio of 32.

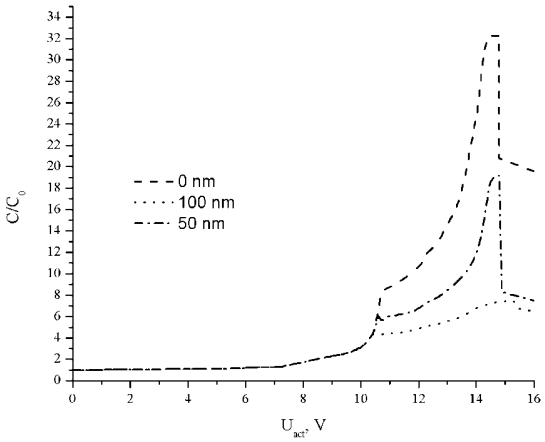

Figure 3: Simulated capacitance depending on the applied voltage. Different lines correspond to the different surface roughness

The capacitance calculated using formula (2) gives a minimum capacitance of 0.061 pF. The maximum calculated capacitance is 2.2 pF with zero air gap which is actually limited by the cantilever and insulator roughness. These results are in an approximate correspondence with simulated value with an error of 8%.

MANUFACTURED MODEL

The developed technology has been adapted for the purposes of manufacturing the RF MEMS 8-bit variable capacitor [6] (Fig.4).

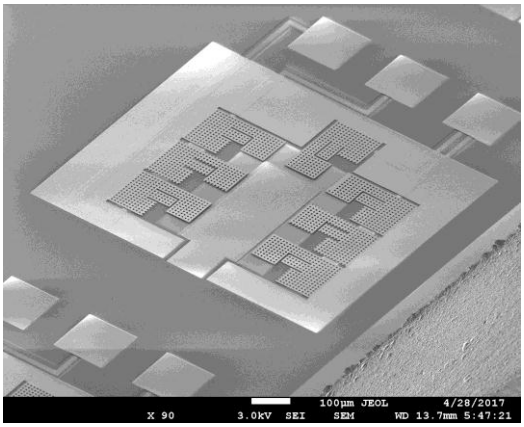

Figure 4: SEM picture of a manufactured 3-bit variable RF MEMS capacitor

7 cantilevers have been designed specificity to maximize the capacitance in an activated state and to smooth the pull-in process, form separate capacitances. By applying 3 different voltages to separate metal pads V1, V2 and V3 (Fig.5), it is able to achieve 8 different capacitance combinations.

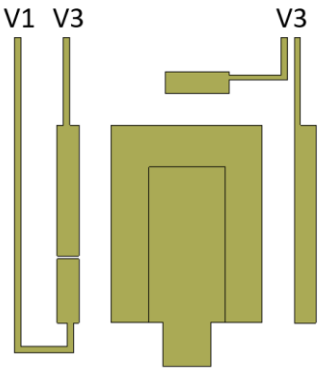

Figure 6: Bottom metal topology of the manufactured capacitor, where V1, V2 and V3 are actuating voltage pads

The main advantage of the presented variable RF MEMS capacitor is an individual cantilever geometry with mechanical supports (Fig.6), which is a subject of the present article. The gap between the movable (cantilever) and static plated of the capacitor is set to be 1 µm which is dictated by the 20 V maximum possible provided value of an actuation voltage. Mechanical simulations provided above shows that the pull-in voltage of the designed cantilever is equal to 14.3 V. Cantilever beam has squared perforations on the suspended parts to allow a uniform etching process of the sacrificial dielectric layer used during the suspended electrode manufacturing.

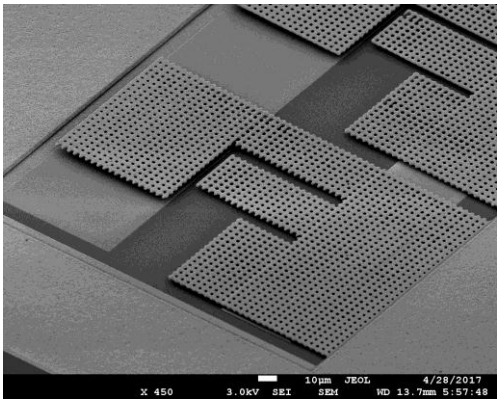

Figure 5: SEM picture of a designed cantilever in an up state

By reviewing the quality of the manufacturing samples, is has been observed that the optimal geometry of the perforation holes is 5x5 µm with a 5µm distance between holes. Smaller holes sizes lead to a more uniform etching of the sacrificial layer while with bigger sizes one can see clear dielectric bumps (Fig.7).

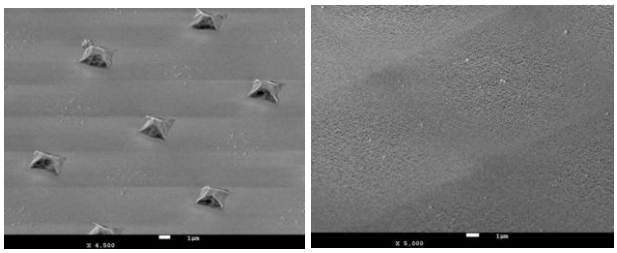

Figure 7: Non-uniformly (left) and uniformly (right) etched sacrificial layer

Measurements confirm the desired performance of the varactor. Fig. 8 presents capacitance dependencies in the wide frequency range for 2 states of the varactor. At the first state, no biasing voltage is applied and all 7 cantilevers are in the up position. Thus, the capacitance is uniform from 2 to 9 GHz and equal to ~1 pF. When V3=15 V is applied (Fig. 5), four cantilevers bend towards the static capacitor edge, thereby increasing the total capacitance. At 9 GHz frequency, the ratio C_{max}/C_{min}=6 is achieved.

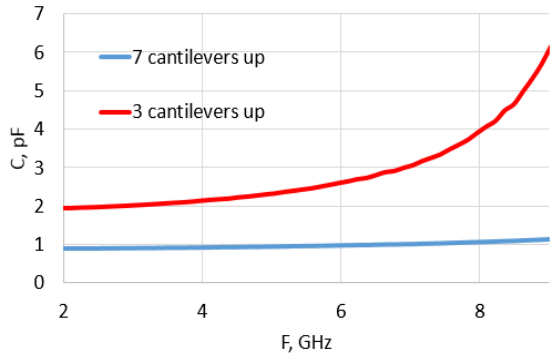

Figure 8: Measured capacitance of the RF MEMS varactors in the frequency range for 2 out of 8 states of the device

Since the capacitance increases linearly with each cantilever, ~ C_{max}/C_{min}=10 ratio can be achieved with all 3 biasing voltages applied.

Thanks to the developed cantilever geometry with mechanical supports, the pull-in process is smooth. In Fig.9 the measured dependence of the capacitance at 9GHz from the applied voltage V3 is shown. When V3>5V, capacitance begins to increase smoothly, which is not common process for the usual RF MEMS capacitance behaviour [7].

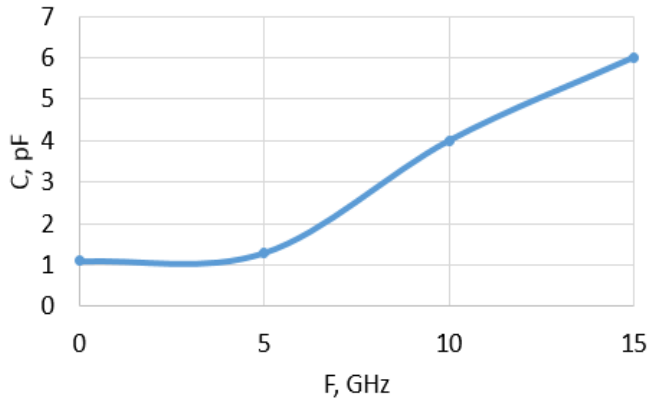

Figure 9: Measured capacitance of the RF MEMS varactors at 9 GHz from the applied voltage to 4 out of 7 cantilevers

CONCLUSIONS

In this paper, we proposed the planar cantilever geometry to be used in RF MEMS switch, where DC biasing voltage electrode is separated from the insulator dielectric area. Thus, the undesirable interaction of dielectric with pull-in voltage is avoided and the problem of dielectric charging and further cantilever adhesion to it is avoided. However, shifting biasing electrode further from the free cantilever edge reduces the lever and requires higher voltage value to achieve the pull-in state. To decrease this value and increase the capacitance switching coefficient, we designed the cantilever geometry with additional mechanical suspensions to distribute the attraction force smoothly around the cantilever contact area and provide smooth pull-in process. Finite element simulations show than the smooth process is achieved and pull-in voltage equals to 14.3 V and capacitance switch ratio is 32. We have also demonstrated that due to the realistic roughness, nonlinear effect of the capacitance dependence on voltage is decreasing along with C_{max}/C_0 ratio.

Designed cantilever was manufactured as a part of an 8-bit RF MEMS capacitor. Measurements show the smooth capacitance changing from the applied biasing voltage along with a big C_{max}/C_{min} value.

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